YIKANG OUYANG

PhD Student ⋄ Microelectronics Thrust
The Hong Kong University of Science and Technology (Guangzhou)
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RESEARCH INTERESTS

- Electronic Design Automation (EDA), AI-aided VLSI design,VLSI modeling and optimization

EDUCATION

The Hong Kong University of Science and Technology (Guangzhou), China Aug. 2022 – present
Ph.D. student Microelectronics

Sun Yat-Sen University, Guangzhou, China Sep. 2018 – Jul. 2022
B.Eng. Microelectronics

AWARDS AND HONORS

[A1] **Best Paper Award**, ACM/IEEE International Workshop on Machine Learning for CAD (MLCAD), 2023.

[A2] Full Postgraduate Scholarship, HKUST(GZ), 2022-present.

PROJECTS

Logic Synthesis Modeling and Optimization Multi-Task Learning Guangzhou, China
Advisor: Prof. Yuzhe Ma *Sep 2022 – Present*
The Hong Kong University of Science and Technology (Guangzhou)

- Proposed a multi-task learning model to predict circuit delay and area.
- Explore Parato-optimal synthesis commands.
- Use LLM for synthesis sequence optimization.

Mask Optimization in VLSI Manufacturing Guangzhou, China
Advisor: Prof. Yuzhe Ma *Aug 2022 – Nov 2022*
The Hong Kong University of Science and Technology (Guangzhou)

- Use ResNet to predict mask offsets to optimize design quality.

Multiplier Design Guangzhou, China
Advisor: Prof. Yuzhe Ma *Sep 2022 – Dec 2022*
The Hong Kong University of Science and Technology (Guangzhou)

- Design multipliers with different encodings and structures.

PUBLICATIONS

Journal Papers

[J1] Xiaoxiao Liang, Yikang Ouyang, Haoyu Yang, Bei Yu, **Yuzhe Ma**, "RL-OPC: Mask Optimization with Deep Reinforcement Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 43, no. 01, pp. 340–351, 2024.

Conference Papers

[C2] Yikang Ouyang, Sicheng Li, Dongsheng Zuo, Hanwei Fan, **Yuzhe Ma**, "ASAP: Accurate Synthesis Analysis and Prediction with Multi-task Learning", ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Utah, Sep. 2023. **(Best Paper Award)**

[C1] Dongsheng Zuo, Yikang Ouyang, **Yuzhe Ma**, "RL-MUL: Multiplier Design Optimization with Deep Reinforcement Learning", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, Jul. 09-13, 2023.

SKILLS

- Language: English, Chinese, Cantonese

- Programming Language: Python, C/C++, MATLAB
- Hardware Design Language: Verilog, CHISEL